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SURFACE TRANSPORT STUDIES FOR MOS DEVICES.(U)

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SURFACE TRANSPORT STUDIES FOR MOS DEVICES

FINAL REPORT

R. S. Muller

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Three topics concerned with conduction in inversion channels at a silicon surface were investigated. One was an experimental investigation of the behavior of free-carrier velocities in surface inversion layers as functions of fields normal and tangential to the inversion channel. Another was the study of DMOS (double-diffused MOS) transistors to clarify the behavior of conduction mechanisms in novel forms of these devices. The novel DMOS structures were studied because they offered processing advantages. Also there was an investigation into the mechanisms of hot carrier injection into silicon dioxide under surface avalanche-breakdown conditions.

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STATEMENT OF PROBLEMS STUDIED

Three topics concerned with conduction in inversion channels at a silicon surface were investigated.

1. An experimental investigation of the behavior of free-carrier velocities in surface inversion layers as functions of fields normal and tangential to the inversion channel.

2. A study of DMOS (double-diffused MOS) transistors to clarify the behavior of conduction mechanisms in novel forms of these devices. The novel DMOS structures were studied because they offered processing advantages.

3. An investigation into the mechanisms of hot carrier injection into silicon dioxide under surface avalanche-breakdown conditions.

Summaries of research results in these three areas have appeared in the five semi-annual Progress Reports that were prepared during the course of this contract period.

BRIEF SURVEY OF IMPORTANT RESULTS

1. Extensive experimental studies of the variation of surface velocities when tangential and normal fields are changed has been carried out. Both p- and n-type silicon substrates with (111) and (100) orientations were investigated. The measurements obtained have been fit empirically to a universal curve which is specified by three parameters. The formula used is

$$v = \frac{\mu_0 \varepsilon}{(1+(\varepsilon/\varepsilon_{crit})^{\alpha})^{1/\alpha}}$$

Values for α, ε_{crit} and μ_0 have been obtained and tabulated. By presenting the results in this form, the research becomes useful directly to device and circuit designers for accurate modeling of MOS transistors and other devices that depend on the precise control of surface conduction. Measurements have also been carried out as a function of temperature for all of the orientations and doping types. A full theoretical treatment establishing the validity of the measurement scheme has been completed and discussed in conference presentations. Two journal articles giving the experimental results and showing the theoretical models are in preparation for publication in Solid-State Electronics. A doctoral thesis by Richard Coen has been completed which fully describes this research. This research has produced the most thorough information on carrier mobilities and velocity saturation at an inverted silicon surface that is yet available.

2. Models for DMOS transistors have been evolved that have clarified the performance to be expected from these devices and have provided a guide to several aspects of their design. This study also showed that applications of DMOS technology could be made in order to permit a simpler complementary MOS (CMOS) process than is provided by conventional processing.

3. Conduction in short-channel MOS devices is only partially characterized by an understanding of free-carrier transport at the surface. The process of charge injection from silicon into silicon dioxide is becoming recognized as one of the important determinants of the ultimate performance of these devices. Charge injection has been studied intensely in our work through use of novel gated-diode structures. We have carried out experiments and developed theory that has resulted in an increased understanding of a number of features of avalanche charge injection. Specifically, we have investigated the localized nature of charge injection into the oxide. We have also carried out research that identifies the nature of surface traps which act to limit the injected currents. We have shown how the techniques

evolved can be used to obtain a continuous display of the flat-band voltage at a surface under conditions of continued surface avalanche. From this instrumentation, we have evolved means to determine the trapping characteristics of bulk oxide states as well as of surface states.

PUBLICATIONS LIST

A. Papers in Refereed Journals

1. T. Masuhara and R. S. Muller, "Complementary DMOS Process for LSI," IEEE Journal of Solid-State Circuits, v. SC-11, pp. 453-458, August 1976.

2. R. Amantea and R. S., "Studies of Localized Charge Injection in Surface-Avalanched pn Junctions," Proceedings of the Eighth Conference on Solid-State Devices, Tokyo, 1976; Japanese Journal of Applied Physics, v. 16, 1977, Supplement 16-1, pp. 205-210.

3. T. Masuhara and R. S. Muller, "Analytical Techniques for the Design of DMOS Transistors," Proceedings of the Eighth Conference on Solid-State Devices, Tokyo, 1976; Japanese Journal of Applied Physics, v. 16, 1977, Supplement 16-1, pp. 173-178.

B. Conference Papers

1. "Complementary DMOS Process for LSI," paper 24.1 at the International Electron Devices Meeting, Washington, D. C., 1-3 December 1975.

2. "Studies of Localized Charge Injection in Surface-Avalanched pn Junctions," paper A3-9 at Eighth Conference on Solid-State Devices, Tokyo, Japan, 1-3 September 1976.

3. "Analytical Techniques for the Design of DMOS Transistors," paper A3-4 at Eighth Conference on Solid-State Devices, Tokyo, Japan, 1-3 September 1976.

4. "Experimental Determination of Carrier Velocities in Inverstion Layers on Silicon," presented at the Solid-State Device Research Conference, Cornell University, Ithaca, New York, 27-29 June 1977.

5. "The Effects of Charge Injection on Gated-Diode Breakdown," presented at the Solid-State Device Research Conference, Cornell University, Ithaca, New York, 27-29 June 1977.

Three additional publications covering details of the research described in conference papers 4 and 5 are in preparation at the present time.

SCIENTIFIC PERSONNEL SUPPORTED BY THIS PROJECT AND DEGREES AWARDED

1. Robert Amantea: Ph.D. to be awarded December 1977.

Thesis: "Studies of Avalanche Injection of Charge into SiO_2 Using Gated Diode Structures" (abstract appended).

Mr. Amantea was an RCA Fellow — research partially supported.

2. Richard Coen: Ph.D. to be awarded December 1977.

Thesis: "Velocity of Surface Carriers in Inversion Layers on Silicon" (abstract appended).

3. Chi Chang: M.S. to be awarded December 1977.

4. Toshiaki Masuhara: Carried out research in support of his Ph.D. degree at University of Kyoto, Japan, September 1976.

Thesis: "Studies on Low Voltage - Low Power MOS Devices for Digital Integrated Circuits."

STUDIES OF AVALANCHE INJECTION OF CHARGE INTO

SiO_2 USING GATED DIODE STRUCTURES

Dep't of Electrical Engineering and Computer Science

PhD Robert Amantea

Richard S Muller Chairman

ABSTRACT

New types of gated diodes have been designed to obtain information concerning the injection of hot carriers into silicon dioxide under avalanche conditions. These devices permit one to determine many properties of the Si-SiO_2 system as a function of time. For example, experiments with one of these devices (a gated diode with an asymmetrically split gate) have shown that there is a transient movement of the centroid of avalanche injection after the start of avalanche. We use this information to generate a model for gated-diode breakdown that includes the effects of trapping of avalanche-injected charge in the oxide. The model clearly demonstrates the critical parameters of the structure. In particular we show that the breakdown voltage V_{BR} for gated diodes with thin oxides is given by

$$V_{BR} = V_{BRO} - V_G$$

where V_G is the gate voltage with respect to the substrate and V_{BRO} is the initial breakdown voltage of the diode when the gate is shorted to the substrate.

This model is then used to explore the relationship between avalanche injection and the trapping of avalanche-injected charge in the oxide. We show that avalanche injection follows a thermal emission process in which the emitted electrons are characterized by a very high effective temperature. Furthermore, the relationship between the breakdown

voltage and the gate voltage implies that shifts in the flat-band voltage due to charge trapping in the oxide result in an equal change in the breakdown voltage, that is $\Delta V_{BR} = \Delta V_{FB}$. Thus, the shift in breakdown voltage is directly related to the oxide trapping parameters. We use this result to determine the capture cross-sections of electron traps in the oxide. It is shown that the initial rate of change of V_{BR} can be useful as a quality factor for the oxide.

Another result that follows from our gated-diode model is the theoretical prediction that the magnitude of the avalanche-injected oxide current depends upon the surface-state charge. Specifically, we show that the transient oxide current decay is due to hole trapping at the Si-SiO$_2$ interface. We develop a model for this phenomenon that is similar to the model used to study the effects of radiation on MOS devices. A method for estimating the density of hole traps at the interface is demonstrated.

This work makes clear the usefulness of gated diodes as diagnostic devices for MOS processing and for device-reliability studies.

VELOCITY OF SURFACE CARRIERS IN INVERSION

LAYERS ON SILICON

Richard William Coen

Ph.D.

Dept. of Electrical
Engineering and
Computer Science

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Chairman of Committee

ABSTRACT

Velocity-field curves for surface free-carriers in silicon have been determined from measurements on resistive-gate IGFETs. Since carrier velocity in the channel of an IGFET is influenced not only by the field tangential to the channel, but also by the field normal to it, a family of velocity-field curves have been measured. Each member of the family gives velocity versus the tangential field at a fixed value of the normal field.

A discussion is given of the conditions under which the channel in a resistive-gate IGFET is uniform. The analysis includes the effect of the ionized impurities (bulk charge) on the channel charge and the effect of the location of the contacts to the gate resistor on the gate bias. We also discuss several experiments which are used to measure various properties of the IGFET such as channel length and width, threshold voltage, insulator capacitance, etc.

The velocity-field measurements were performed on n-channel devices fabricated on both (100) and (111) substrates and on p-channel devices

fabricated on (100) substrates. The channel length of the devices was $\sim 8\ \mu m$ and the impurity concentration of the substrates was $\sim 10^{15}\ cm^{-3}$. Measurements were made for tangential fields between 5×10^2 and 2×10^4 volts/cm. The corresponding velocities were between 10^5 and 6×10^6 cm/sec. For tangential fields below $\sim 8 \times 10^3$ volts/cm the velocity-field curves exhibit constant mobility. At higher fields, the curves depart from the low-field asymptote and velocity approaches a limiting value. For both carrier types, velocity decreases as the normal field increases. Values for the saturation velocity have been obtained by curve-fitting the experimental data to a phenomenological velocity-field relationship. The saturation velocity of electrons is found to be between 5×10^6 and 6×10^6 cm/sec for both (100) and (111)-oriented silicon. The saturation velocity for holes is found to be between 1.5×10^6 and 2×10^6 cm/sec.